REMARKS

Claims 1-9 are pending in this application of which claims 1, 3 and 5 are independent. Following response to the restriction requirement, claims 3-6 and 8-9 have been withdrawn, and claims 1, 2, and 7 examined. Claims 1 and 2 have been amended. Reconsideration in light of the following remarks is respectfully solicited.

The Examiner objects to Figs. 7(a)-7(c), as these figures are not designated as prior art. Moreover, it was noted that Fig. 8 should be designated as prior art. Correction to these figures has been made and is submitted concurrently herewith. Withdrawal of the drawing objection is respectfully solicited.

Also, the Examiner objects to Figs. 1(a)-1(b), 3(a)-3(b), 5(a)-5(b), and 7(a)-7(b), and alleges that there is no brief description of these drawings in the specification. In order to correct this discrepancy, certain paragraphs spanning pages 9 and 10 within the section entitled "Brief Description of the Drawings" have been amended to appropriately reference each drawing subset, and is believed to overcome the drawing objections posed by the Examiner. Withdrawal of these objections is respectfully solicited.

The Office Action rejects claim 1 under 35 U.S.C. § 112. Claim 1 has been amended to replace the term "the width" on lines 14, 15 and 17 with the term --a width-- in order to satisfy antecedent basis for each limitation. Also, the Examiner indicates that the term "the drain line" in line 15 lacks antecedent basis. However, proper antecedent basis is found in line 11 of claim 1. It is believed that all indefiniteness problems have been addressed and overcome. Withdrawal of the rejection is respectfully solicited.

The Examiner rejects claims 1, 2, and 7 under 35 U.S.C. § 103(a) as being unpatentable over Shiga [et al.], (U.S. Patent No. 6,476,418) in view of Tsujimura [et al.] (U.S. Patent Application No. 2001/0043292 A1). The rejection is respectfully traversed.

The Office Action relies on Shiga for illustrating a plurality of gate lines (102), a plurality of source lines (line including electrode 106), a gate insulating film (103), a thin film transistor, a semiconductor layer (104), and a pixel electrode (107). The Examiner alleges that Shiga discloses the requirement of claim 1 that recites "a width of a crossing portion of the semiconductor layer . . . that cross[es] an edge line of the gate electrode [is] made smaller than a width of the drain electrode . . . ." Applicants disagree.

As seen in each of the plan views (Fig. 1(a), Fig. 4(a), and Fig. 6(a)), in Shiga, the semiconductor layer 104 has a width that is *greater* than the width of a crossing portion of the semiconductor layer that crosses an edge of the gate electrode 102 (see Fig. 1(a)), or the semiconductor layer 104 *terminates* at a crossing portion of an edge of the gate electrode 102 (see Figs. 4(a) and 6(a)). There is no disclosure or suggestion that a width of a crossing portion of a semiconductor layer that *crosses* an edge line of the gate electrode is *smaller* than that of the drain electrode, as claim 1 recites.

Referring to the Office Action, the Examiner relies on Fig. 6(a) of Shiga as illustrating this claim limitation, and characterizes the claimed gate electrode as the photo carrier generating regions 109. The Examiner's characterization is believed to be improper. Referring to column 3, lines 48-64 of Shiga, it is explained that the semiconductor layer *terminates* at the edge of the gate electrode 102 so as to create photo carrier generating regions 109 adjoining the drain electrode 106a and the source electrode 106b, such that the gate electrode 102 is not shielded by semiconductor layer 104. Thus, contrary to the Examiner's assertion, Fig. 6(a) does not illustrate "a width of a crossing portion of the semiconductor layer 104 that crosses an edge line of the gate electrode 102," as claim 1 recites, because the semiconductor layer 104 terminates at the edge portion of the gate electrode 102.

The Examiner acknowledges that Shiga does not disclose "a width of a crossing portion of . . . a drain line that cross[es] an edge line of the gate electrode [is] smaller than that of the drain electrode," as claim 1 recites, to which Applicants agree. However, the Examiner alleges that Tsujimura discloses this feature, and that "it would have been obvious . . . to employ Shiga et al. [with this feature] in order to minimize a leakage current in a floating island region formed in a TFT." The Examiner has not established a *prima facie* case of obviousness.

First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine the teachings. The Examiner bases motivation on the desirability to minimize a leakage current in a floating island region formed in a TFT. Floating island regions may be formed in top-gate structures as shown in Tsujimura but not in bottom-gate structures as shown in Shiga. More specifically, referring to Figs. 7 and 8 of Tsujimura, a floating island region is formed by an exposed region of the gate insulating film 107 and a-Si film 106 (see Fig. 8) so as to increase the distance between the gate electrode 108 and source and drain electrodes 105, 104. As a result, short-circuiting due to surface leakage may be prevented (see paragraphs 8 and 9 of Tsujimura). However, disadvantageously, current in the floating island region may be uncontrollable. In order to lessen the effects of the floating current, Tsujimura shortens the channel length (distance between the drain electrode 15 and source electrode 14), L_{on}, in the region where the TFT actually operates (a range covered by the gate electrode 18), and lengthens the channel length in the floating island region 22 related to the generation of off-current L_{off}, as seen in Fig. 1. As a result, leakage current caused by the floating island region 22 may be reduced to negligible levels (see paragraph 52 of Tsujimura).

On the contrary, there is no disclosure or suggestion in Shiga of a floating island region formed in the TFT. Because Shiga is a bottom-gate electrode, there is no short-circuiting between the gate electrode 102 and other electrodes 106a, 106b, as the semiconductor layer 1, 2 or 3 completely covers gate electrode 102 (see section views Figs. 1(b), 4(b), and 6(b) of Shiga). As a result, there would be no reason to create a floating island region in Shiga. Thus, motivation based on minimizing leakage current in a floating island region in Shiga, the primary reference that would be modified, asserted by the Examiner, is not applicable.

Secondly, there must be a reasonable expectation of success for the proposed combination. The Examiner has not established how the proposed combination of Shiga and Tsujimura would successfully minimize a leakage current in the floating island region formed in the TFT. Shiga does not have a floating island region, as discussed above. Moreover, Shiga is a bottom-gate electrode structure whereas Tsujimura is a top-gate electrode structure and they are not combinable. It is not clear how one would combine the teachings, and moreover, if the combination was made, whether it would be successful following the proposed modification.

Finally, the prior art references when combined must teach or suggest all of the claim limitations. However, as addressed above, Shiga fails to disclose "a width of a crossing portion of the semiconductor layer . . . that cross[es] an edge line of the gate electrode [is] made smaller than the width of the drain electrode . . .," as claim 1 recites. Also, Tsujimura has been thoroughly reviewed, yet there is no discussion or suggestion of a width of the semiconductor layer at the crossing portion, as claim 1 requires. Thus, the combination of the references fails to teach or suggest all of the claim limitations of claim 1.

For the above-discussed reasons, the Examiner has failed to establish a *prima facie* case of obviousness. Claims 2 and 7 are patentable at least based on dependency to claim 1 and for the reasons discussed above. Withdrawal of the claim rejection is respectively solicited.

If the Examiner has any comments or questions regarding this response or the Application in general, the Examiner is encouraged to contact the undersigned in order to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Encl: 2 Replacement Drawings

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Date: January 5, 2004